Sub :- Power Electronics SYEJ

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Class Test 1. Model Answer.

Q. 1]

i] Draw the labeled V-I characteristics of power transistor.

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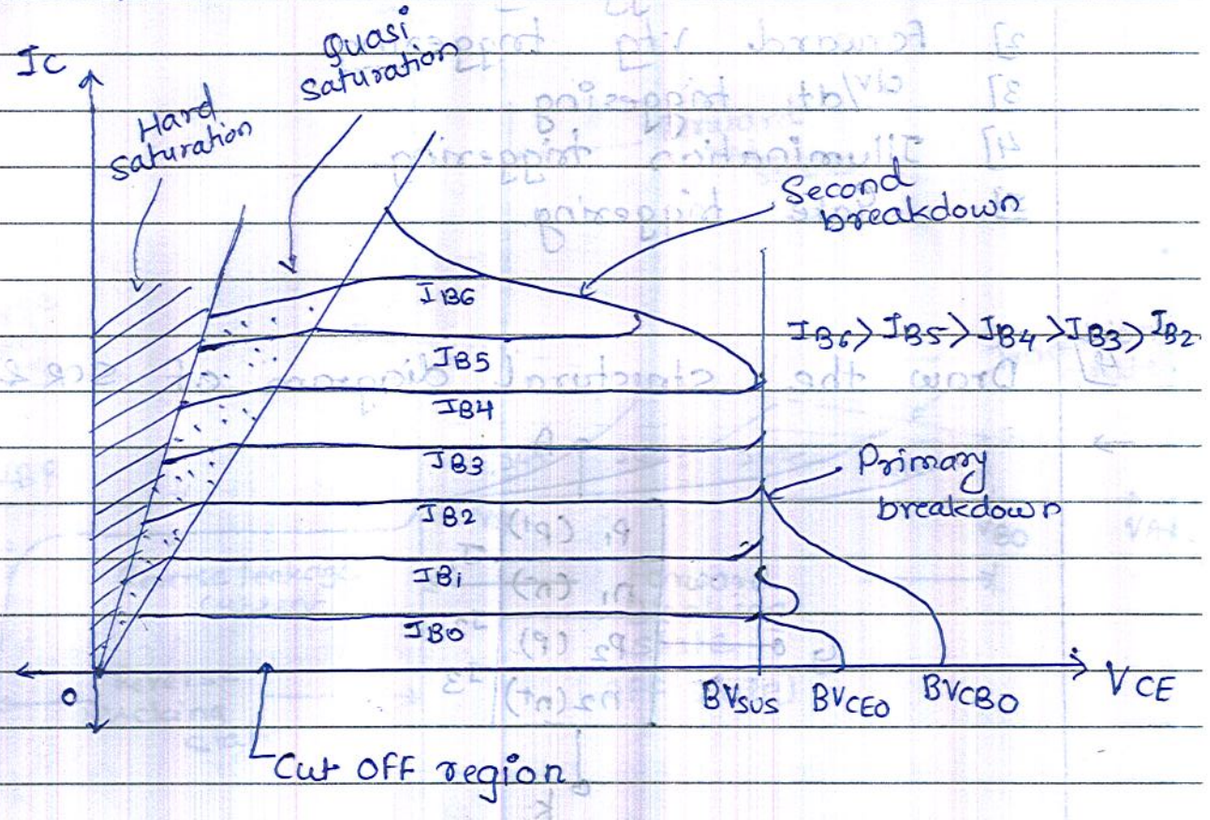

2] Draw the symbols of following devices.

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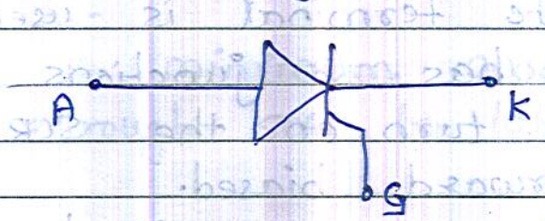
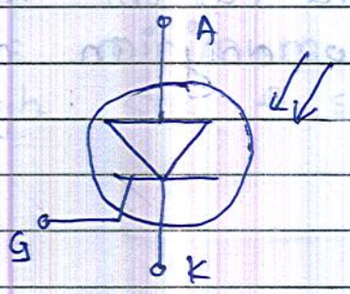
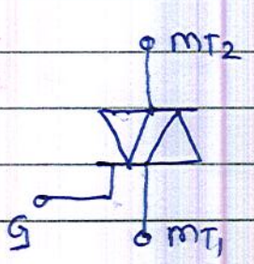
i] SCR →



ii] LASCR →



iii] TRIAC →



3] List the different turn off on methods of SCR.

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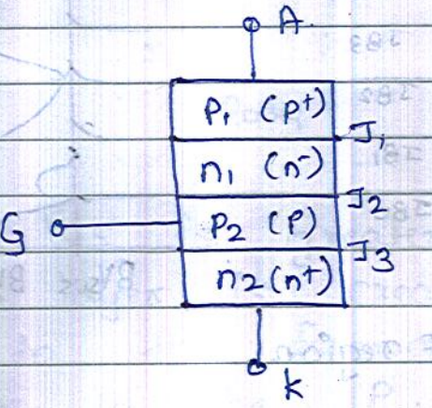
1] Thermal triggering
2] Forward v/g triggering
3] dv/dt triggering
4] Illumination triggering.
5] Gate triggering.

4] Draw the structural diagram of SCR & explain.

→



- It is a 4 layer PNPN structure.
- It has 3 terminals, anode, cathode & Gate.
- Gate terminal is used to turn on the SCR.
- It has 3 junctions like J_1, J_2 & J_3.
- To turn on the SCR, SCR must be in forward biased.
- SCR is a unidirectional device.
- Gate current is only positive i.e. it can flow only in one direction.

Q. 2]

i] Draw the V-I characteristics of SCR. Define latching current & holding current.

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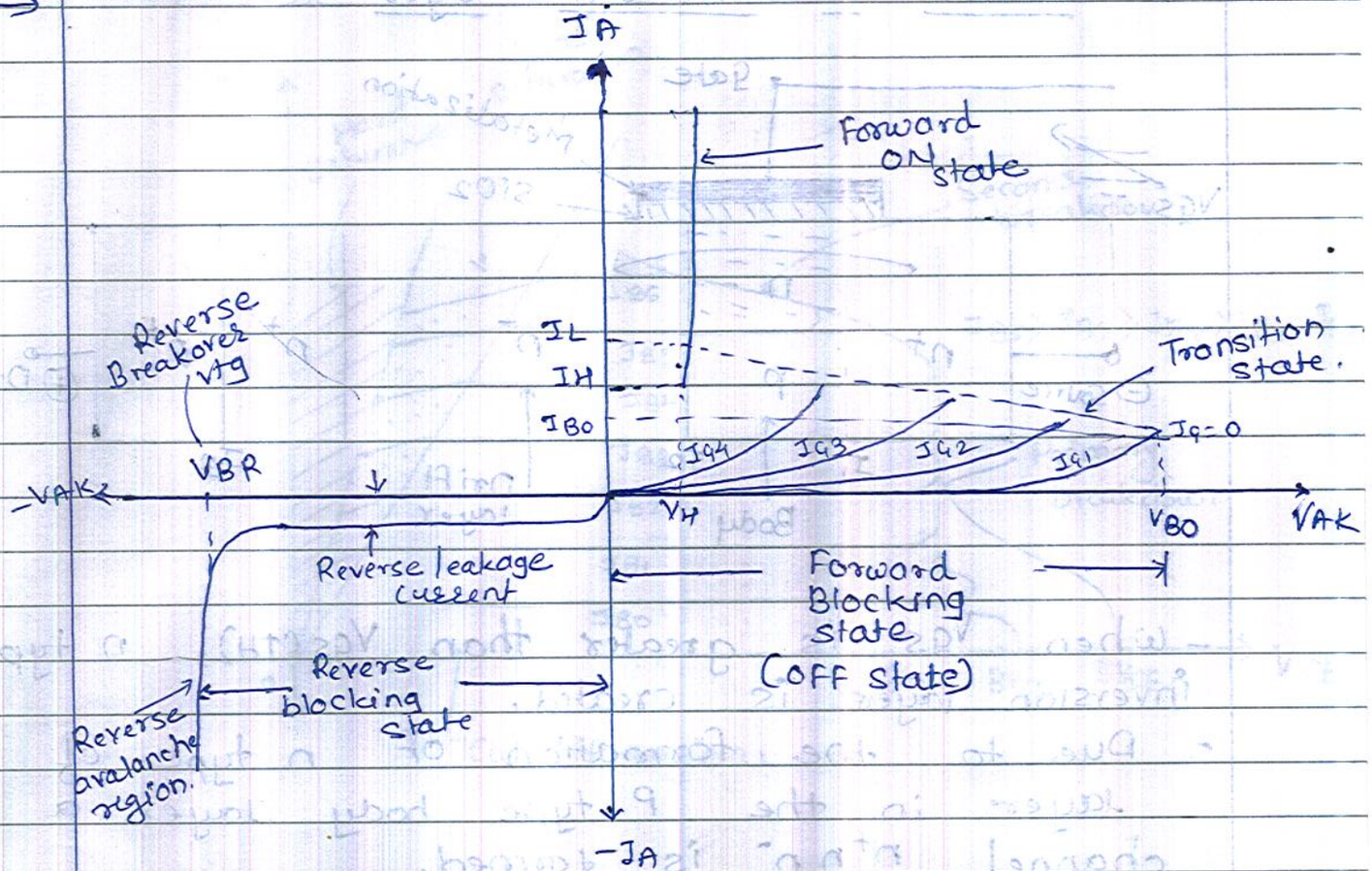


Latching current (I_L) :-

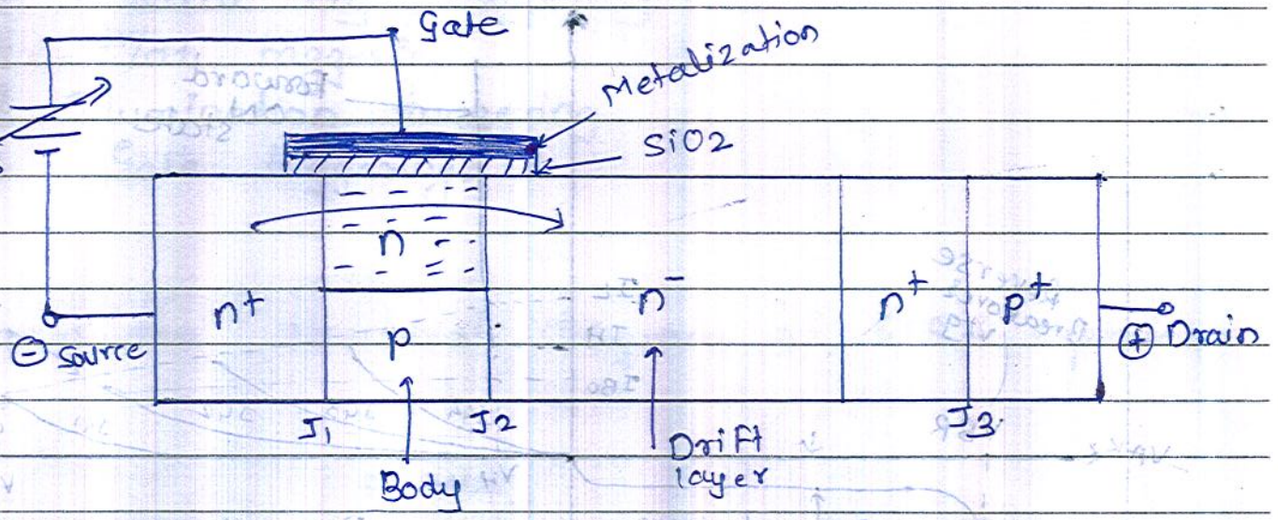
It is minimum anode current that must flow through SCR to latch it into the on state.

Holding current (I_H) :-

It is minimum current that can flow through SCR & still hold it in the on state.

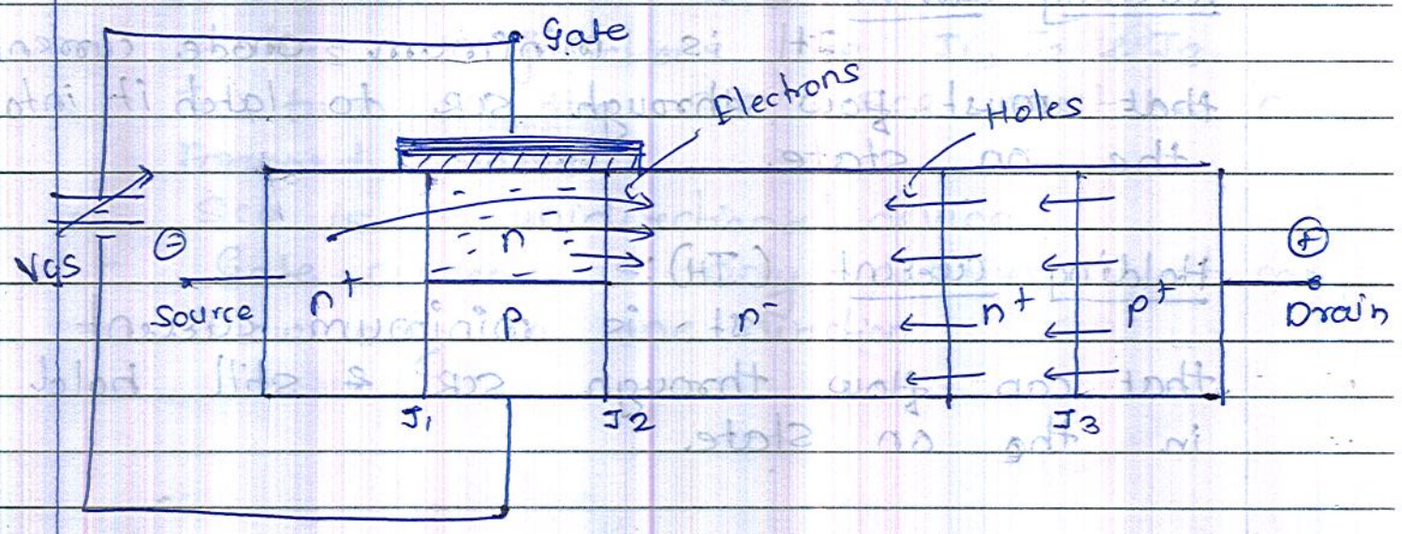
2] Explain the operating principle of IGBT.

→ i] Creation of inversion layer.



- When V_{GS} is greater than $V_{GS(TH)}$, n type inversion layer is created.
- Due to the formation of n type of layer in the P type body layer a channel $n^+ n n^-$ is formed.

ii] Conductivity Modulation :-



- When the forward vltg betⁿ drain & source is applied, junction J_3 is forward biased.
- Due to creation of inversion layer electrons from the source are injected into the n^- drift layer via $n^+ p n^-$ i.
- As the J_3 is forward biased, it will inject holes in the n^+ buffer layer. The electrons injected in the n^- drift layer create a space charge which will attract holes from the n^+ buffer layer which were injected by p^+ layer.
- So the double injection takes place into the n^- drift region from both sides.
- This increases the conductivity of the drift region & reduces the resistance to its minimum.

3] Explain dv/dt triggering of SCR.

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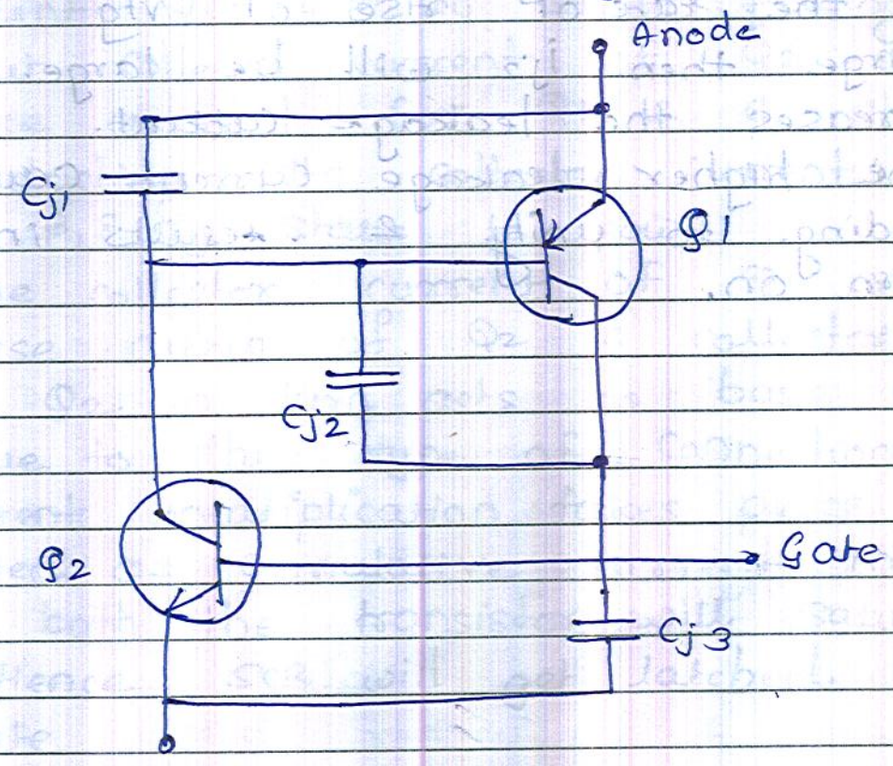

- Assume that $I_G = 0$, & suddenly apply a very high forward vtg bet^n anode & cathode of a thyristor.
- Then it is said that rate of change of voltage i.e. dV/dt.
- Such a situation is called as transient operating condition.

- The current through C_{j2} is

$$I_{j2} = \frac{d(q_{j2})}{dt} = \frac{d}{dt}(C_{j2} V_{j2})$$

$$= V_{j2} \frac{d C_{j2}}{dt} + C_{j2} \frac{dV_{j2}}{dt}.$$

where

- C_{j2} - capacitance of J_2
  V_{j2} - voltage of J_2
  q_{j2} - charge in the junction.

- If the rate of rise of vtg dV/dt is large then i_{j2} will be large. & this increases the leakage current.
- The higher leakage current causes $(\alpha_1 + \alpha_2)$ tending to unity & results in SCR turn on.

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Q.3

1] Explain the two transistor analogy of SCR.

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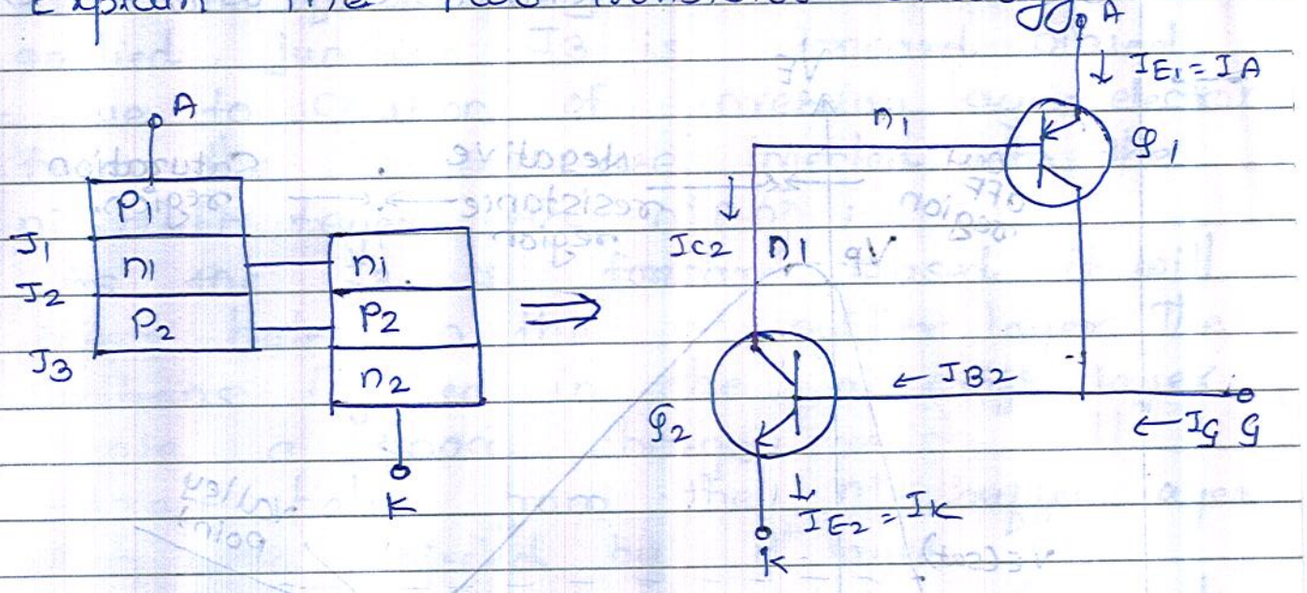

- The equivalent ckt is made up of p-n-p & n-p-n transistor.
- The anode is +ve w.r.t. cathode. & gate current is supplied.
- The gate current acts as base current for Q_2 & it turns on. Its collector current $I_{C2} = \beta_2 I_G$ starts flowing.
- But collector current of Q_2 acts as base current for Q_1 & Q_1 starts conducting. Its collector current $I_{C1} = \beta_1 I_{B1} = \beta_1 \beta_2 I_G$ starts to flow.
- The collector current of Q_1 acts as base current of Q_2 & collector current of Q_2 in turn acts as base current of Q_1.
- Due to this type of connection, the current multiplication takes place which is called as cumulative current multiplication. & both the transistor will saturate.
- Hence SCR will get latched into on state.

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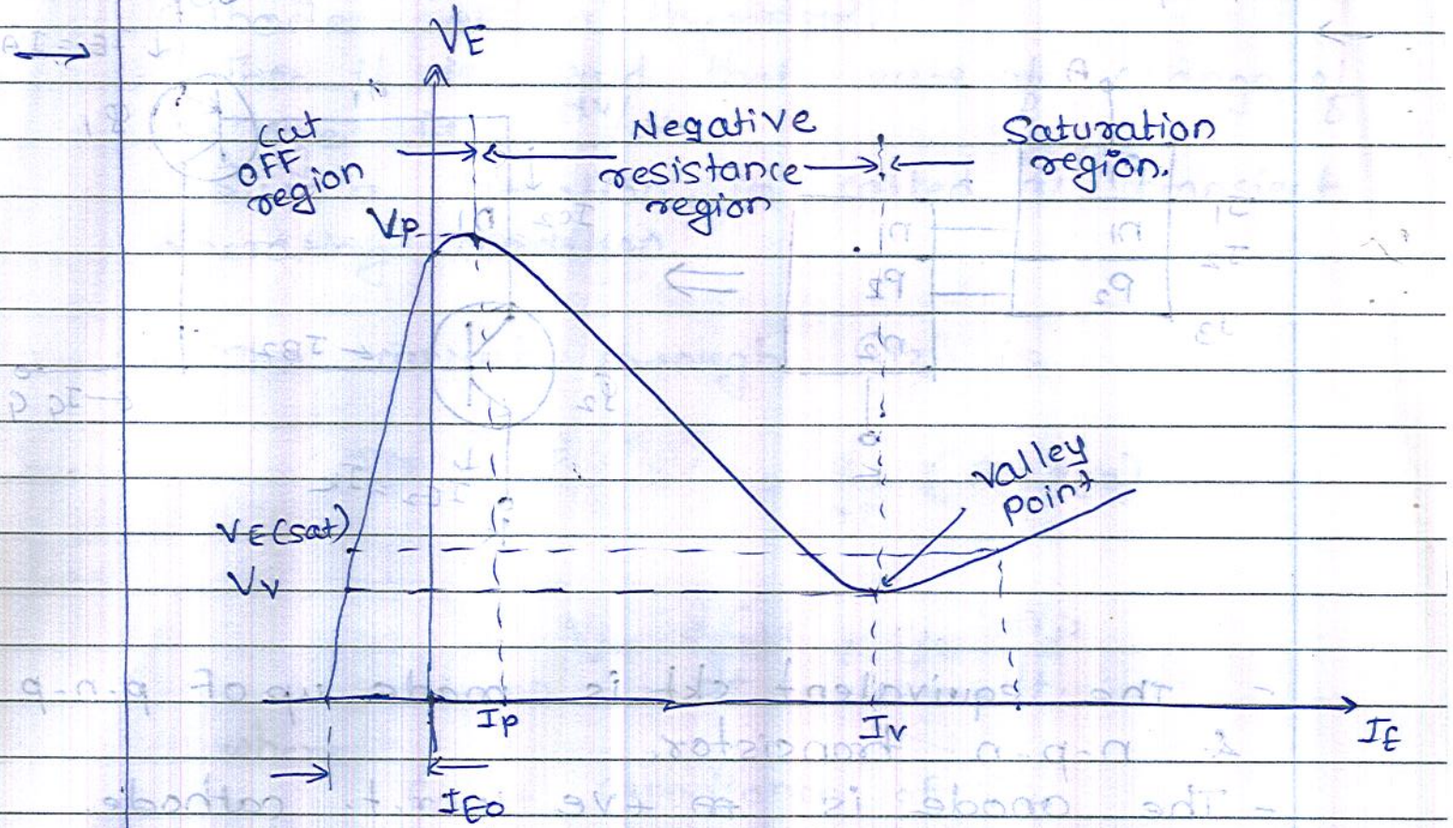
b] Draw the V-I chara. of UJT & explain.



- This is a emitter vtg versus emitter current characteristics.
- When emitter vtg less than the V_p UJT is in the OFF state & I_E is not greater than I_{EO}.
- The I_{EO} corresponds to reverse leakage current. This region is known as cut off region.
- As the emitter vtg. increases & reaches V_p, the UJT starts conducting.
- Then with increase in emitter current I_E the emitter vtg decreases.
- This region of operation is known as negative resistance region.
- Eventually the valley point will be reached & a further increase in I_E will place the device into saturation.

3] Explain the resistance triggering circuit for SCR.

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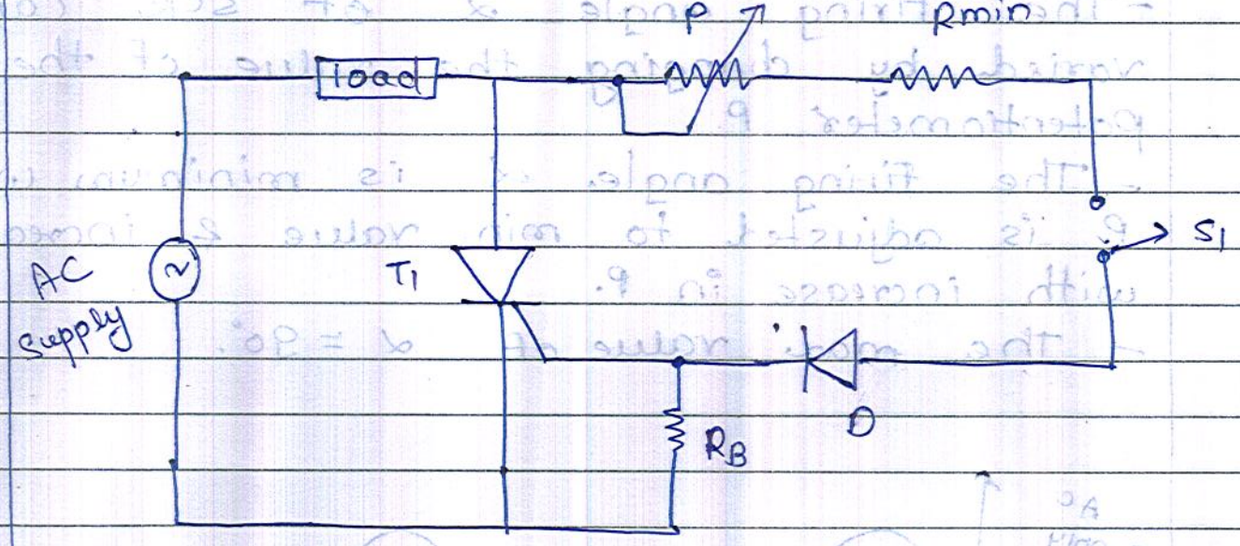
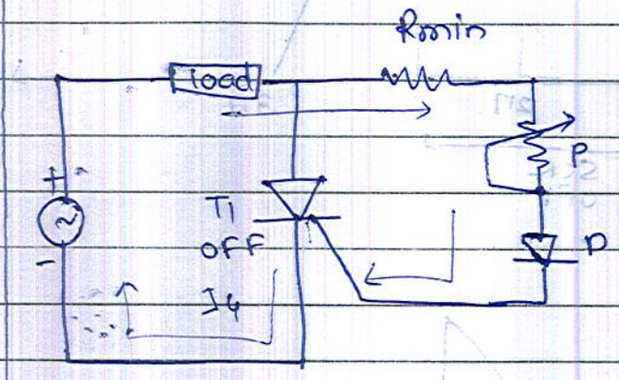
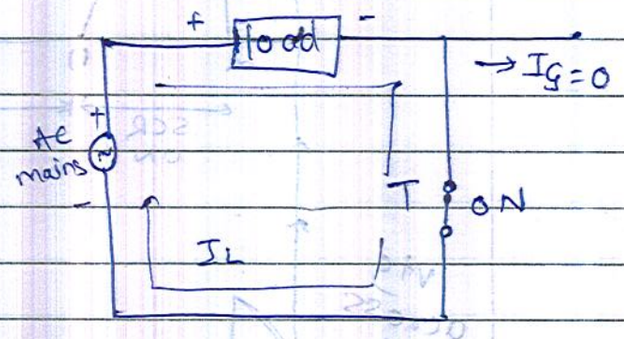


- In above ckt dia. 'P' decides the value of peak gate current. The diode D is used to prevent reverse voltage from being applied across the gate cathode junⁿ.



SCR OFF



SCR ON.

- In the +ve half cycle of AC supply, the current flows through P, D, Rmin & gate cathode junⁿ of SCR.
- When SCR is turned ON, the vtg across it reduces to its conduction drop value, at very small value. The gate current is then almost zero.

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- The SCR continues to conduct upto π radians. if load is purely resistive.
- The Firing angle α of SCR can be varied by changing the value of the potentiometer P.
- The Firing angle α is minimum when P is adjusted to min. value & increases with increase in P.
- the max value of α = 90°.